al., claims 12-15 under §103(a) over Han et al and Arakawa in view of Waki et al., claims 16, 18 and 19 under §103(a) as being unpatentable over Han et al., and claim 17 under 103(a) as being unpatentable over Han et al., and further in view of Su et al. The rejections under are fully traversed below. Reconsideration of the application is respectfully requested based on the following remarks.

Claims 20-25 have been canceled. Claims 1-19 are now pending in this application.

ELECTION/RESTRICTION

The Applicant hereby affirms the election of group I, claims 1-19.

REJECTION OF CLAIMS 1-19 UNDER 35 U.S.C. §103

Independent claims 1 and 7 of the present invention require bonding wires that are specifically "stitch bonded" to the bond pad of a semiconductor die. As is generally known in the industry, stitch bonding involves bonding a wire to a contact point in which the point of a capillary through which the wire is extruded is pressed onto the contact point such that the extruded wire is caught between the contact point and the point of the capillary. Then, the capillary is pressed onto the contact point with sufficient force so that the extruded wire is snipped off and remains bonded to the contact point. As discussed in the specification, stitch bonding to the bond pads on the semiconductor die of claims 1 and 7 is advantageous in that the wire loop height over the die is minimized. In turn, the minimized wire loop height allows the resulting semiconductor device package to have a smaller thickness.

Han et al. describes attaching bonding wires to semiconductor die in very general terms such as "putting on" bonding wires. *See* col. 2, line 34, and col. 4, line 42. However, Han et al. does not teach or suggest that the wires are "put on" in any specific manner, whether by stitch bonding or ball bonding. As such, Han et al. does not teach or suggest stitch bonding a bonding wire to the bond pad of a die nor does it teach or suggest techniques for minimizing the wire loop height over a die in a packaged device.

Similarly, Arakawa and Waki et al. also do not teach or suggest use of "stitch bonding." First, Arakawa discusses a wire bonding technique that utilizes a wire cut damper 5 (*see* figure 3) that cuts a wire like a pair of scissors would. However, Arakawa does not teach or suggest the use of stitch bonding, which snips a wire in the manner discussed above. Second, Waki et al. is directed towards connecting semiconductor die to contact leads using tape leads instead of wires.

As such, Waki et al. also does not teach or suggest the use of stitch bonding. Therefore it is respectfully submitted that the cited references, alone or in any combination, do not teach or suggest the semiconductor device package as recited in claims 1 and 7.

Independent claim 12 also pertains to a semiconductor device package having a bonding wire that is stitch bonded to a semiconductor die. However, claim 12 also requires that the stitch bond is attached to a conductive ball formation that is on top of the bond pad of the semiconductor die. The conductive ball formation is especially advantageous because it creates a protective buffer so that the surface of the semiconductor die does not get damaged by the capillary, which presses down upon the die in order to create the stitch bond. As discussed with respect to claims 1 and 7, none of the cited references teach or suggest the use of a stitch bond. It follows then that none of the cited references teach a stitch bond that is created upon a conductive ball formation that is on a semiconductor die. Therefore it is respectfully submitted that the cited references, alone or in any combination, do not teach or suggest the semiconductor device package as recited in claim 12.

Independent claim 16 also pertains to a semiconductor device package with a bonding wire that is stitch bonded to a semiconductor die. Additionally, the bonding wire is stitch bonded to a contact lead. Stitch bonding a wire to both a die and a contact lead avoids the use of ball bonding techniques which tend to have relatively large loop heights. (Typically, current practices ball bond an interconnecting wire to a contact lead.) In contrast, in addition to not teaching or suggesting a stitch bond created on a die, the cited references do not teach or suggest stitch bonding a wire to both a die and a contact lead. Furthermore, claim 16 requires that the bonding wire is stitch bonded to the contact lead before it is stitch bonded to the die. This requirement further ensures that the loop height of the wire over the die is minimized since the loop height near the first stitch bond is typically smaller than the loop height near the second stitch bond. The cited references clearly do not teach this additional requirement that the bonding wire be stitch bonded to the contact lead before it is stitch bonded to the die. Therefore it is respectfully submitted that the cited references, alone or in any combination, do not teach or suggest the semiconductor device package as recited in claim 16.

It is submitted that dependent claims 2-6, 8-11, 13-15, and 17-19, which depend from claims 1, 7, 12, or 16 are also patentably distinct from the cited references for at least the same reasons as those recited above for their corresponding independent claims. These dependent claims further recite additional limitations that further distinguish these dependent claims from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection

of claims 1-19 under 35 U.S.C § 103(a).

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 500388 (Order No. SDK1P007).

Respectfully submitted,
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